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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PHAM, LY D	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 09/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/729,831	CHEN ET AL	
	Examiner	Art Unit	
	Ly D. Pham	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-151* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11-14,26-44,46-49,61-83,85-88,100-120,122-125 and 137-151* is/are rejected.

7)☒ Claim(s) *10,15-25,45,50-60,84,89-99,121 and 126-136* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *insofar submitted*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Reasons for Allowance*.

DETAILED ACTION

1. Applicants' Pre-Amendment filed June 08, 2004 has been entered. The specification has been amended.

2. Applicants' Information Disclosure Statements, IDS', filed September 23, 2004, March 21, May 31, June 10, and August 29, 2005 have been considered by the Examiner.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 11 – 13, 35, 46 – 48, 74, 85 – 87, and 122 – 124 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In **claims 11, 46, 85, and 122**, the phrase "... such that both **programmed** and unprogrammed memory cells in the unselected NAND string ..." is considered indefinite because there should not be any cell in the unselected string that can be programmed.

Also, in **claim 35 and 74** the "series selection device" is a string selection switch transistor, which is understood not as a memory cell transistor, and consequently cannot be programmed. It can only be turned on or off. Therefore, it is considered unclear how the series selection devices can be programmed to a threshold voltage.

Correction and/or clarification are required in order to overcome this type of rejection.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1 – 9, 14, 27, 36 – 44, 49, 75 – 83, 101, 110, and 112 – 120 rejected under 35 U.S.C. 102(e) as being anticipated by Kanda et al. (US Pat 6,522,583 B2).

Regarding **claims 1 and 36,** Kanda et al. disclose a method of operating an integrated circuit (and its corresponding apparatus for operating the same) having a memory array (figs. 1 or 6, memory cell array 11) including at least one plane of memory cells (figs. 2, 7, or 9), said memory cells comprising switch devices having a charge storage dielectric and which cells are arranged in a plurality of series-connected NAND strings (figs. 2, 7, or 9), said method comprising the steps of:

biasing a channel region of a half-selected memory cell in an unselected NAND string of a selected memory blocks, to a first voltage (col. 3, lines 16 – 22 and col. 5, lines 3 – 32, "... the initial channel potential of a memory cell before channel boost becomes higher than at least VDD – Vth,...". The "VDD being write inhibit level to a cell

unit, ...". Note that in fig. 4, at time t1 to time t2, Vread is applied to all word lines of the selected blocks and VSG is applied to SGD, fig. 2, which permits VDD applied from BL"1" to transfer to the channels of all of the non-selected cells, col. 3, lines 61 – 67, which includes the half-selected cell); and then

capacitively coupling the channel region to a second voltage different than the first voltage when a selected word line associated with the half-selected memory cell transitions to a word line programming voltage (again in fig. 4, from time t2 to time t3, voltage transition from VSG to VDD level applied to SGD in fig. 2 lowers the potential from BL"1" applied to the program-inhibit cells and additionally, at time t3, a program voltage Vpgm is applied to the selected word line, resulting in different biasing conditions to all of the "half-selected" cells, which consequently establishes a second voltage different from the initial voltage to the channel region of the half-selected memory cells. See further col. 6, lines 20 – 60), to thereby reduce a voltage potential between the selected word line and the channel region of the half-selected memory cell.

Regarding **claims 2 – 3, and 37 – 38**, Kanda et al. also disclose the method of claims 1 and 36, wherein the biasing step further comprises decoupling the half-selected memory cell from a bias source/adjacent device channel regions after establishing its channel region to the first voltage—the half-selected memory cell channel region to the first voltage (in fig. 2, since these memory cells are series-connected NAND strings, the channel of one cell inherently couples to the "adjacent cell" in the series". Therefore, after a half-selected memory cell establishes the initial channel voltage during t1 – t2, fig. 4, decoupling from a bias source as a result of VSG

switching to VDD applied to SGD during t2 – t3 decouples the half-selected memory cell from a bias source, and also inherently means from adjacent memory cell).

Regarding **claims 4 and 39**, Kanda et al. also disclose the method as recited in claims 1 and 36, wherein the biasing step comprises:

(a) conveying a bit line inhibit voltage on a respective first array line associated with the unselected NAND string (fig. 2, bit lines bit lines BL0 – BL4 and col. 5, lines 6 – 11 and 26 – 32);

(b) coupling the first end of the unselected NAND string through a first group of at least one series selection device (fig. 2, series selection devices being the selection transistors whose gates are connected to SGD), to the respective first array line associated with the unselected NAND string; and

(c) turning on the half-selected memory cell and any intervening memory cells between the half-selected memory cell and the first end of the unselected NAND string (figs. 2 and 4, Vread turns on the cells along the non-selected word line WL3, two of them being the intervening cells right above the two half-selected cells on the left and the right of the selected cell in BL2); and then

(d) decoupling the channel region of the half-selected memory cell from the respective first array line after establishing the half-selected memory cell channel region to the first voltage (as shown above in claims 2 and 3).

Regarding **claims 5 and 40**, Kanda et al. further disclose the method of claims 4 and 39 wherein the step (c) comprises driving the word lines associated with the half-selected memory cell and any intervening memory cells between the half-selected

memory cell and the first end of the NAND string to a passing voltage sufficient to turn on both programmed and unprogrammed memory cells to bias the half-selected memory cell channel to the first voltage (as discussed above, fig. 4 shows Vread is the passing voltage to turn on both the programmed and unprogrammed memory cells ... See also col. 4, lines 17 – 21 and col. 5, lines 26 – 28).

Regarding **claims 6 – 7, 41 – 42**, Kanda et al. also disclose the method of claims 5 and 40, wherein the first voltae is substantially equal or less than the bit line inhibit voltage (col. 5, lines 6 – 8, VDD of write inhibit level or VDD – Vth, col. 4, lines 7 – 9 and 55 – 60).

Regarding **claims 8 and 43**, Kanda et al. also disclose the method of claims 5 and 40, wherein step (c) further comprises driving all word lines associated with memory cells of the unselected NAND string to the first passing voltage (fig. 4, at time t1, both selected and unselected word lines are applied with Vread—passing voltage as shown above).

Regarding **claims 9 and 44**, Kanda et al. also disclose the method of claims 4 and 39, wherein the (d) comprises turning off at least one memory cell adjacent to the half-selected memory cell (fig. 19 shows a modification where voltages applied to the bit lines of BL"0" and BL"1" being VSS and Vclamp at time t4, which turns of the memory cells adjacent to the half-selected memory cell.

Regarding **claims 14 and 49**, Kanda et al. also disclose the method of claims 4 and 39, further comprising:

(e) coupling a first end of a selected NAND string of the selected memory block through a first group of at least one series selection device (fig. 2, selected NAND string connected to BL2 with one selection switch on top—middle transistor with gate connected to SGD), to a respective first array line (fig. 2, array selection line BLTR) associated with the selected NAND string, said respective first array line conveying a bit line programming voltage (fig. 2, BLTR line turn on the high-voltage type transistor in order for the bit line bias voltages to be conveyed to the bit lines BL0 – BL4... of the block as shown);

(f) coupling the bit line programming voltage to a channel region of a selected memory cell in the selected NAND string, said selected memory cell also associated with the selected word line (fig. 2, string of selected bit line BL2 includes selected cell whose channel is coupled to selected word line WL2, see further col. 3, line 26 – col. 4, line 45 and col. 6, lines 20 – 30).

Regarding **claims 27**, Kanda et al. shows in figs. 1 and 2 the method of claim 1, wherein the memory array comprises a two-dimensional array having one plane of memory cells formed in a substrate (array 11).

As per **claims 75 – 83, 101, and 112 – 120,** the apparatus disclosed therein are considered inherent given the method steps as indicated above.

Regarding **claim 110**, Kanda et al. also show the integrated circuit of claim 75, wherein the memory cell device and series selection devices forming each NAND string are structurally substantially identical (see fig. 2, the strings are shown to be substantially identical).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 26, 61, and 100 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanda et al. in view of Choi et al. (US Pat 6,469,933 B2).

Regarding **claims 26 and 61**, Kanda et al. disclose the method of claims 1 and 36, except further comprising repeating the disclosed steps for a given half-selected memory cell to provide a plurality of programming pulses and to re-establish a voltage bias of the half-selected memory cell channel region before each such programming pulse. However, such feature has been taught by Choi et al. (fig. 1, repeating program pulses, col. 4, lines 19 – 44).

Therefore, it is considered obvious to one of ordinary skill in the art, at the time the invention was made, to incorporate the feature taught by Choi et al. to the disclosure by Kanda et al. so that the flash memory device the program inhibited memory cells is prevented from soft-programming during program operation (col. 2, line 53 – col. 3, line 45).

As per **claim 100**, the apparatus disclosed therein is considered inherent given the method steps as shown above.

9. Claims 28 – 34, 62 – 68, 72, 73, 102 – 108, and 137 – 143 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanda et al. in view of Shimizu et al. (US Pat 6,115,287).

Regarding claims **28, 29, 32, 62, and 65 – 68,** Kanda et al. disclose the method of claims 1 and 36, except wherein the memory array comprises a three dimensional memory array having at least two planes of memory cells formed above an insulating substrate, and wherein the charge storage dielectric comprises an ONO stack, which comprises a floating gate electrode. The features are nonetheless taught by Shimizu et al. (col. 14, lines 49 – 57 and col. 7, lines 31 – 44, ONO insulating film with the Nitride layer being the floating gate electrode).

Therefore, it is considered obvious to one of ordinary skill in the art, at the time the invention was made, to combine the feature taught by Choi et al. to the disclosure by Kanda et al. so that a nonvolatile semiconductor memory device which is improved in element isolation and high-degree of integration is provided (col. 3, lines 7 – 11).

Regarding claims **30, 31, 63, and 64**, Shimizu et al. also disclose the substrate comprising either monocrystalline substrate or polysilicon (col. 14, lines 40 – 48 or col. 25, line 58 – col. 26, line 6).

Regarding **claims 33, 34, 72, and 73**, Kanda et al. also disclose the method of claims 28 and 36, wherein the switch devices comprise transistors having a depletion mode threshold voltage for one of two data states, erased data state and programmed data state (col. 3, lines 3 – 10).

As per **claims 102 – 108 and 137 – 143**, the apparatus disclosed therein are considered inherent given the method steps as shown above.

10. Claims 69, 109, 144, and 149 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanda et al. in view of Forbes (US Pat 6,853,587 B2).

Regarding **claims 69, 109, 144, and 149**, Kanda et al. disclose the method of claim 36 and the integrated circuit of claim 112, except wherein the thin film modifiable conductance switch devices comprises silicon nanoparticles and have more than two nominal values of conductance for storing more than one bit of data per cell. However, these features have been shown by Forbes (col. 7, line 60 – col. 8, line 30 and col. 10, lines 19 – 37 disclose memory transistor comprise silicon nanoparticles, and col. 11, line 55 – col. 12, line 16 show each transistor can store two bits of data storage density).

Therefore, it is considered obvious to one of ordinary skill in the art, at the time the invention was made, to combine the features shown by Forbes to the disclosure by Kanda et al., so that needs for very high density memory storage devices can be met (col. 1, line 29 – col. 2, line 16).

11. Claims 70, 71, 145, and 146 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanda et al. in view of Nazarian (US Pat Pub 2005/0111260 A1).

Regarding **claims 70, 71, 145, and 146**, Kanda et al. disclose the method of claims 36 and the integrated circuit of claim 112, except wherein the thin film modifiable

conductance switch devices comprise a polarizable or ferroelectric material. However, these features have been shown by Nazarian (paragraph 0004, last 4 lines).

Therefore, it is considered obvious to one of ordinary skill in the art, at the time the invention was made, to include the features taught by Nazarian to the teachings by Kanda et al., so that various memory types provide versatility according to specific application requirements and/or needs).

12. Claims 111 and 151 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanda et al.

As per **claims 111 and 151**, the Examiner takes an Official Notice of the claimed feature in which the integrated circuit of claims 75 and 112 embodied in computer readable descriptive form suitable for design, test, or fabrication of the integrated circuit, to be considered common and well-known in the art as microelectronic designs, as well as the majority of almost all other studies are done using computer systems for speed, managerial and neatness purposes.

Allowable Subject Matter

13. **Claims 10, 15 – 25, 45, 50 – 60, 84, 89 – 99, 121, and 126 – 136** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

14. The following is a statement of reasons for the indication of allowable subject matter:

The prior arts fail to teach or suggest:

The method of claim 4 or 39, and its apparatus for operating the same, as set forth in claims 84 or 121, wherein step (d) comprises turning off at least one device within the first group of at least one series selection device of the unselected NAND string.

Or The method of claim 14 or 49, further comprising:

(g) turning off at least one device of a second group of at least one series selection device at a second end of the unselected NAND string opposite the first end, ...; and

(h) turning off at least one device of a second group of at least one series selection device at a second end of the selected NAND string opposite the first end, ...

15. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

17. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02(b)).

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ly D. Pham whose telephone number is 571-272-1793. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho can be reached on 571-272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ly D. Pham
September 2, 2005

HUAN HOANG
PRIMARY EXAMINER